Systems and Methods for Holdover Circuit for Phase Locked Loops

Abstract of the Disclosure

Improved phase locked loops are described which handle momentary breaks in an input communication channel. The phase locked loops provide the capability to "hold" the output clock in a communication system at or very near the last output frequency before the loss of input data. The phase locked loops according to the teachings of the present invention include a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal. An electronic selector circuit is coupled to a differential output of the phase detector with an input that is responsive to a detected state of the input signal. An operational amplifier based loop filter circuit is provided in the phased locked loop. The electronic selector circuit provides the differential output of the phase detector at a pair of inputs to the operational amplifier. A voltage controlled oscillator is coupled to an output of the operational amplifier and provides an output frequency for the phased locked loop circuit. The electronic selector circuit is operable to control the input to the operational amplifier to hold an output frequency of the voltage controlled oscillator at a substantially constant frequency. In one embodiment of the present invention, the electronic selector circuit includes a switch which couples the pair of inputs together when a reference signal, or input signal to the phase detector is interrupted. In another embodiment of the present invention, the electronic selector circuit includes a logic-based selector circuit which holds the pair of inputs to an identical potential level when the input signal to the phase detector is interrupted. Systems and methods are further included within the scope of the present invention.

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